

## CLAIMS

What is claimed is:

- 1    1.    A method of processing a predicated instruction comprising:  
2            receiving a consumer instruction in an reservation station of an out-order  
3    processor;  
4            receiving a predicated instruction in the reservation station, wherein the  
5    consumer instruction depends on a result of the predicated instruction;  
6            dispatching the predicated instruction to an execution unit;  
7            executing the predicated instruction; and  
8            storing the executed predicate instruction in a re-order buffer.
- 1    2.    The method of Claim 1, wherein dispatching the predicated instruction to an  
2    execution unit includes stalling the predicated instruction until all non-predicated  
3    dependencies are resolved.
- 1    3.    The method of Claim 1, further comprising:  
2            resolving the predicate of the executed predicate instruction;  
3            dispatching the consumer instruction to an execution unit; and  
4            executing the consumer instruction.
- 1    4.    The method of Claim 1, further comprising updating a resolved status of the  
2    predicated instruction after the predicate is resolved.
- 1    5.    The method of Claim 4, wherein the resolved status of the predicated

2 instruction is updated in a scoreboard.

1 6. The method of Claim 4, further comprising:

2 dispatching a consumer instruction after the predicate of the predicated

3 instruction is resolved; and

4 executing the consumer instruction.

1 7. The method of Claim 6, further comprising.

2 storing the result of the predicated instruction in a register, if the predicate is

3 true; and

4 deleting the result of the predicated instruction in a register, if the predicate is

5 not true.

1 8. A method of processing a predicated instruction comprising:

2 receiving a predicated instruction in an execution stage of an in-order pipeline;

3 stalling the predicated instruction until predicate is resolved;

4 storing the result of the predicated instruction in a register, if the predicate is

5 true; and

6 deleting the result of the predicated instruction, if the predicate is not true.

1 9. The method of Claim 8, further comprising:

2 determining if a predicated instruction is followed by a consumer instruction

3 in the next clock cycle, wherein the consumer instruction depends on a result of the

4 predicated instruction; and

5 slipping the predicated instruction to a previous stage in the pipeline if the

6     predicated instruction is not followed by the consumer instruction in the next clock  
7     cycle.

1     10.     The method of claim 9, wherein the predicated instruction is followed by a  
2     consumer instruction in the next clock cycle further comprising:

3             storing the predicated instruction in an associative buffer;  
4             resolving the predicate; and  
5             executing the consumer instruction.

1     11.     A computer system comprising:

2             a processor, wherein the processor includes:

3                 a plurality of dynamic pipeline stages including at least one predicated  
4             instruction;

5                 a register renaming unit;

6                 a reorder buffer;

7                 a plurality of execution units; and

8                 a plurality of reservation stations wherein the register renaming unit,

9     the reorder buffer, the plurality of execution units and the plurality of

10    reservation stations are coupled to at least one of the plurality of dynamic

11    pipeline stages, wherein:

12                 the predicated instruction is received in at least one of the

13             plurality of reservation stations;

14             the predicated instruction is dispatched to the execution unit;

15             the predicated instruction is executed in the execution unit; and

16             a result of the executed, predicated instruction is stored in the

1    12.    The system of Claim 11, further comprising a scoreboard.

1     14.     A computer system comprising:  
2             a processor, wherein the processor includes:  
3                     a plurality of in-order pipeline stages including at least one predicated  
4             instruction and a consumer instruction and wherein:

5                   the predicated instruction is received in an execution stage of  
6                   the pipeline;  
7                   if the predicated instruction is not followed by the consumer  
8                   instruction in the next clock cycle then the predicated instruction is  
9                   slipped to a previous stage in the pipeline;  
10                  if the predicated instruction is followed by the consumer  
11                  instruction in the next clock cycle then  
12                  stalling the predicated instruction until predicate is

13 resolved; and  
14 storing the result of the predicated instruction in a register, if  
15 the predicate is true; and  
16 deleting the result of the predicated instruction, if the predicate  
17 is not true.  
18 a system bus;  
19 a computer memory system; and  
20 an input/output device, wherein the system bus is coupled to the processor, the  
21 computer memory system and the input/output device.

1 15. The system of Claim 14, wherein the memory system includes an associative  
2 buffer coupled to the pipeline.

1 16. The system of Claim 15, storing a predicated instruction in the associative  
2 buffer until a consumer instruction occurs in the next in clock cycle.